

ABSTRACT OF THE DISCLOSURE

Provided are semiconductor devices having a system-on-chip (SOC) configuration that combines both a capacitor-based cell-array memory region and one or more MOS core/peripheral circuit/logic regions on a single chip and a method for manufacturing such devices. The manufacturing process reduces the number of additional photolithographic processes required and modifies the relationship between the sizing of various layers and/or structures to reduce the fabrication cost and improve the reliability of the resulting devices. In particular, the capacitors for the memory region are formed in the same insulating layer as the first metal pattern for the core/peripheral circuit/logic regions of the devices, thereby producing capacitors and metal patterns of substantially the same height and thickness respectively. A landing structure may also be formed in the cell array region in combination with the first metal pattern for improving the contact process in the cell array region.